IN THE CLAIMS

Please amend claim 1 as follows:

1(Amended). A memory cell, comprising:

providing a PMOS drive transistor with a gate terminal, a first source/drain terminal, and a second source/drain terminal;

providing a NMOS pass transistor with a gate terminal, a first source/drain terminal and a second source/drain terminal wherein a current flowing through the source/drain terminals of the NMOS pass transistor is greater than a current flowing through the source/drain terminals of the PMOS drive transistor for the same voltages applied between the gate and source/drain terminals of the PMOS drive transistor and the gate and source/drain terminals of the NMOS pass transistor ;

connecting said first source/drain terminal of said NMOS pass transistor to a bitline;

connecting said second source/drain terminal of said NMOS pass transistor to a first storage node;

connecting said gate terminal of said NMOS pass transistor to a wordline;

connecting said first source/drain terminal of said PMOS drive transistor to a supply voltage;

connecting said second source/drain terminal of said PMOS drive transistor to said first storage node; and

connecting said gate terminal of said PMOS drive transistor to a second storage node.